REMARKS

By this Amendment, the title and claims 1, 2, 9, 11 and 12 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as its invention. The applicant respectfully submits that no new matter as been added. It is believed that this Response is fully responsive to the Office Action dated April 2, 1999.

The title of the invention is objected to by the Examiner as being non-descriptive. Applicant respectfully asserts that the amendment to the title obviates the objection. Accordingly, withdrawal of the objection to the title of the invention is respectfully solicited.

As to the Merits:

Claims 1 - 14 stand rejected under 35 U.S.C. § 103(a) based on **Uehara et al.** in view of **Hayden**.

This rejection is respectfully traversed.

In the present invention, the contact hole is opened to position the ends of the contact hole over the adjacent two conductor patterns, and then the sidewall insulation film is formed on the inside wall of the contact hole so as to relax patterning size of the photo resist film, and to restrain fluctuations of the contact hole size caused by the alignment error in the photolithography step. Thus,

the semiconductor device which is fabricated by the above-described method has structural characteristics as follows.

I. The end of the contact hole is positioned over the conductor pattern, or is defined by the conductor pattern.

II. The sidewall insulation films are formed in the contact hole on the side walls of the inter-layer insulation film, the side walls of the conductor pattern, and the side walls of the etching stopper film.

In the claimed invention of the present application, these characteristics are clarified. In claims 1, 9, 11, and dependent claims thereof, the end of the contact hole is positioned over the conductor pattern (which includes the word line and the bit line), and the sidewall insulation films are formed in the contact hole on the side walls of the inter-layer insulation film (which includes the first and the second insulation film), the side walls of the conductor pattern, and the side walls of the etching stopper film. In claims 2, 12, and dependent claims thereof, the end of the contact hole is defined by the conductor pattern (which includes the word line and the bit line), and the sidewall insulation films are formed in the contact hole on the side walls of the inter-layer insulation film (which includes the first and the second insulation film), the side walls of the conductor pattern, and the side walls of the etching stopper film.

With respect to **Uehara**, the Examiner asserts that **Uehara** discloses in Fig. 6 a semiconductor device having a base 10; two conductor patterns 50b; a protective etch stopper film covering the upper surface of the patterns 18x; a first insulation film 32; a contact hole between the two conductor patterns; sidewall insulation films 20a, 20b; and a plug buried in the contact hole 50a.

However, **Uehara** does not disclose or fairly suggest the features as now set forth independent claims 1, 2, 9 11 and 12.

That is, while **Uehara** may disclose in Fig. 6 a contact hole, the region where the withdrawn electrode 31 and the buried layer 33 are formed, and an insulation film 32, **Uehara** does not disclose that the withdrawn electrode 31 is formed in the insulation film 32 by etching the insulation film 32.

Moreover, **Uehara** does not disclose or fairly suggest that the sidewall insulation films (20a,20b) are formed on the inter-layer insulation film 32 in the contact hole. **Uehara** also does not teach or suggest the insulation film having substantially the same height as the etching stopper film (protecting film 19).

Furthermore, the Examiner asserts that the dummy electrodes 50b of **Uehara** correspond to the conductor patterns of the claims of the present application. However, dummy electrodes 50b are not adjacent to each other since gate electrode 50a is disposed between dummy electrodes 50b.

In addition, the Examiner asserts that the gate electrode 50a corresponds to the plug buried in the contact hole. However, the gate electrode 50a is not the plug, and is not buried in the contact hole.

With respect to **Hayden**, the Examiner asserts that **Hayden** discloses the use of sidewalls and the protective layer on conductive patterns and refers to this protective layer as an etch stop layer 20.

However, such teachings, even if disclosed in **Hayden**, would still not supplement the above discussed deficiencies or drawbacks in the teachings of **Uehara** in failing to fully meet the claimed invention. Thus, the present invention would not have been unobvious to one of ordinary skill in the art at the time the invention was made based on **Uehara** and **Hayden**, singly or in combination.

Additionally, in **Hayden**, sidewall 32 and 36 are formed after forming the contact hole. However, the sidewall 32 or 36 are formed of the conducting film so that the sidewall 32, 36 of Hayden are clearly different from the side wall insulation film of the claims of the present application and do not provide any motivation for the present invention.

Thus, it is respectfully asserted that the prior art fails to teach or suggest recitations of claims 1, 2, 9, 11 and 12 requested that the Examiner allow these claims, along with the entire application, to issue. Accordingly, withdrawal of the rejection of claims 1 - 14 under 35 U.S.C. §103(a) is respectfully solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
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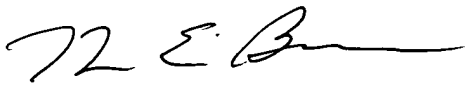

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